User Manual

PE11S100X SERIES
Synthesizer

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Notices

Manual Part Number

PE11S100X SERIES

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- Use this device with the cables provided.
- Do not attempt to service this device. This device should be returned to Pasternack for any service or repairs.
- Do not open the device.

User Environment

This instrument is designed for indoor use only.

Revision Control

Revision	Description of Changes	Date
1.0	Initial Creation	08/18/2011
1.1	Pasternack Updates	05/13/2019

Acronyms

PPL Phase Lock Loop
SCPI Standard Commands for Programmable Instrumentation

Contents

1.0 Applicable Products

PE11S1001, PE11S1002

2.0 General Description

This operating guide applies to the PE11S100X synthesizer modules operating up to 20 GHz output frequency. The purpose of this guide is to describe features common to all the synthesizer modules.

The PE11S100X synthesizer modules contain phase locked loops consisting of various Pasternack die. Additionally, the voltage inputs are internally regulated with low dropout linear voltage regulators.

The PE11S100X synthesizer modules features frequency hopping and frequency sweep functions. The built-in linear sweeper function performs frequency chirps with a wide variety of sweep times, polarities and dwells, all with an external, automatic or software driven sweep trigger. The external trigger signal is sent to the module via the GPIO3 pin.

3.0 Reference Input

The crystal reference input stage is shown in Figure 1. This is a common-emitter single-ended bipolar buffer. Expected input is a 0 dBm sinusoid from a 50 Ohm source. The buffer input impedance is dominated by a 25 Ohm shunt resistor in series with a 50 pF on-chip capacitor. The reference path phase noise floor is approximately equivalent to -159 dBc/Hz. For best performance care should be taken to provide a crystal reference source with equivalent or better phase noise floor.

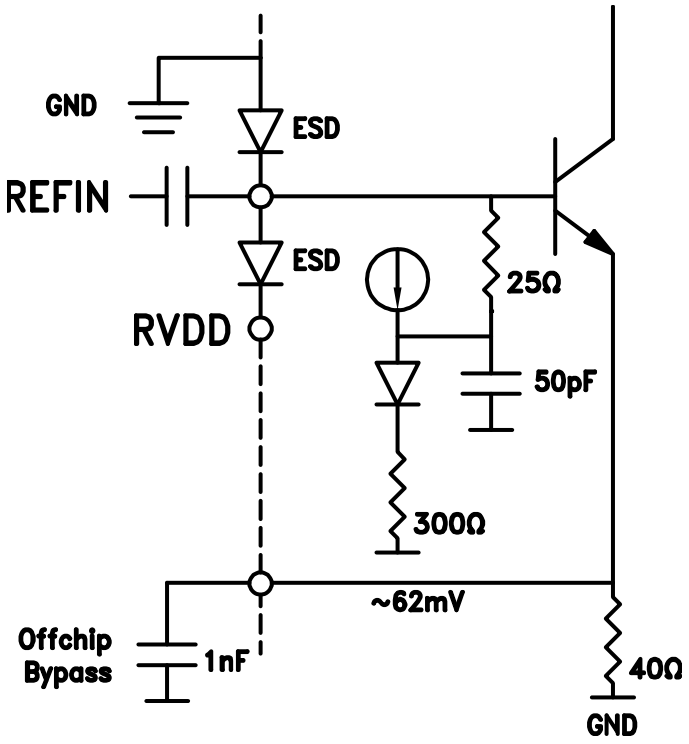

Figure 1. REFIN Input

4.0 Basic Operation

4.1 Initialization

The PE11S100X synthesizer does not maintain register states after power down. After power is supplied to the PE11S100X synthesizer modules, all registers should be loaded with the appropriate values. Default values for these registers can be found in section 7.1 Register Map on page 22, with instructions for performing the serial data write operations found in 5.2 Serial Port WRITE Operation on page 15.

4.2 Frequency Tuning

$$f_{VCO} = f_{REF} \cdot N_{int} \cdot M + \frac{f_{REF} \cdot N_{frac} \cdot M}{2^{24}} \qquad \text{(EQ 1)}$$

Where:

- N_{int} is the integer division ratio, between 36 and 65531 in fractional mode between 32 and 65535 in integer mode
- N_{frac} is the functional division ratio between 0 and 2_{24}-1
- f_{REF} is the frequency of the reference (f_{REFIN}/R), where f_{REFIN} is the reference input frequency.
- M is the prescaler coefficient for the particular synthesizer

As an example, for a synthesizer with M = 2 and f_{REF} = 10 MHz, the output frequency of 4,600,000,001.19 Hz is achieved using N_{int} = 230 and N_{frac} = 1. These are set by programming the 6-bit binary value of 230d =00E6h = 0000 0000 1110 0110 into dsm_intg in Reg 0Fh. Similarly the 24 bit binary value of 1d = 000001h = 0000 0000 0000 0000 0000 0001 into dsm_frac in Reg 10 h.

In integer mode the synthesizer step size is fixed to M times phase frequency detection (PFD) the reference frequency, f_{REF}. Integer mode typically has lower phase noise for a given reference frequency than fractional mode. In integer mode the digital $\Delta\Sigma$ modulator is normally shut off. To run in integer mode set dsm_integer_mode (Reg 12 h<3>) and clear dsm_rstb (Reg 01h<13>). Then program the integer portion of the frequency, N_{int}, as explained by (EQ 1), ignoring the fractional part. From the above example, operation in integer mode would result in a frequency of 4600 MHz.

4.3 Frequency Hopping

If the synthesizer is in fractional mode, a write to the fractional frequency register. Reg 10h will initiate the frequency hop on the falling edge of the 31st clock edge of the serial port write (see Figure 5).

If the integer frequency register, Reg 0Fh, is written when in fractional mode, the information will be buffered and only executed when the fractional frequency register is written.

If the synthesizer is in integer mode, a write to the integer frequency register, Reg 0Fh, will initiate the frequency hop on the falling edge of the 31st clock edge of the serial port write (see Figure 5).

4.4 CW Sweeper Mode

The internal PLL features a built-in frequency sweeper function, useful for test instrumentation, FMCW sensors, automotive radars, and other applications.

Sweeper modes include:

a. Single-Step Ramp Mode

b. 1-Way Sweep Mode

c. 2-Way Sweep Mode (alternating positive and negative frequency ramps)

The sweep generator is enabled with ramp_enable in Reg 14 h<1>. The sweep function cycles

through a series of discrete frequency values, which may be:

a. Single-stepped by individual triggers if ramp_singlestep (Reg 14 h<6>) is set, or

b. Stepped by an automatic sequencer if ramp_singlestep (Reg 14 h<6>) is cleared

Triggering of sweeps, or of steps in single-step mode, may be configured to operate as follows:

a. Triggered from TTL input on GPIO3 if Reg 14 h<5> = 1, or

b. Triggered by setting ramp_trigg (Reg 14 h<2>), if ramp_trigg has previously been cleared, or

c. Triggered with an automatically-generated internal trigger, if ramp_repeat_en

(Reg 14 h<3>) is set.

The sweep will begin at the current frequency value of the synthesizer, denoted as f0. The frequency step size for the ramp is set by ramp_step (Reg 15 h), with

$$\Delta f_{step} = \text{ramp\_step} * f_{REF} / 2^{24}$$

The total number of ramp steps taken in a single sweep is given by ramp_steps_number (Reg 16 h), and the initial ramp direction is set to be increasing or decreasing in frequency by clearing or setting ramp_ startdir_dn (Reg 14 h<4>) respectively. Setting ramp_singledir (Reg 14h<7>) restricts the direction of the sweep to the initial sweep direction only.

The final ramp frequency, ff, is given by $f_f = f_0 + \Delta f_{step}$ * ramp_steps_number for increasing frequency ramps and $f_f = f_0 - \Delta f_{step}$ * ramp_steps_number for decreasing-frequency ramps. Unless in single-step mode, the sweeper timebase, TREF, is the period of the divided reference f_{REF} at the phase detector. So in and the total time to ramp from f_0 to f_f is $T_{ramp} = T_{REF}$ * ramp_steps_number.

The user should be aware that the synthesized ramp is subject to normal phase-locked-loop dynamics. If the loop bandwidth in use is much wider than the rate of the steps, then the locking will be very fast and the ramp will have a staircase shape. As the update rate approaches the loop bandwidth, the loop will not fully settle before a new frequency step is received. In this case, the swept output will have a small lag and will sweep in a near-continuous fashion.

4.4.1 One-Way Sweeps

One-way sweeps are selected by enabling ramp_singledir (Reg 14h<7>). At the end of the ramp time, T_{ramp}, the sweeper will dwell at the final frequency, f_f, until a new trigger is received. The second trigger will hop the synthesizer back to the initial frequency, f_0. The third trigger will restart the sweep from f_0.

So odd-numbered triggers will start a new ramp in the same direction as the initial ramp and even-numbered triggers will hop the synthesizer from the current frequency to f_0 where it will wait for a trigger to start a sweep. Note that the odd-numbered triggers should be timed appropriately to allow the VCO to settle after the large frequency hop back to the start frequency.

The functions of the sweep parameters for one-way sweeps are shown graphically in Figure 2.

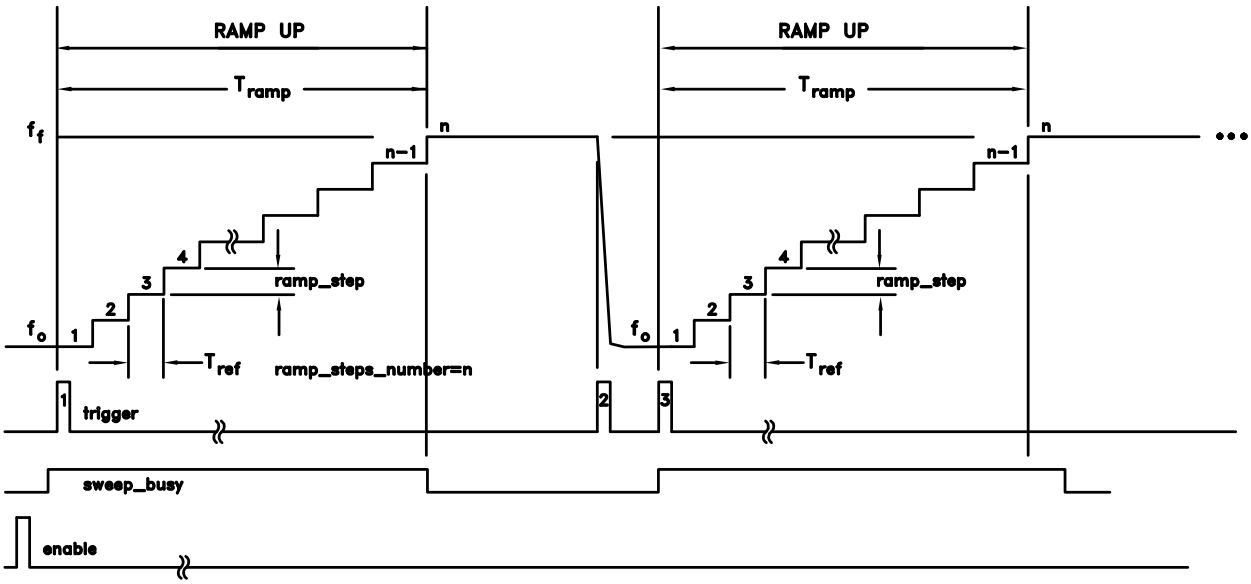

Figure 2. 1-Way Sweep Control

4.4.2 Two-Way Sweeps

If ramp_singledir (Reg 14 h<7>) is disabled, at the end of the ramp time, T_{ramp}, the sweeper will dwell at the final frequency, f_f, until a new trigger is received. This new trigger will reverse the current sequence, starting from f_f and stepping back to f_0. Odd triggers will ramp in the same direction as the initial ramp, while even triggers will ramp in the opposite direction.

The functions of the sweep parameters for two-way sweeps are shown graphically in Figure 3.

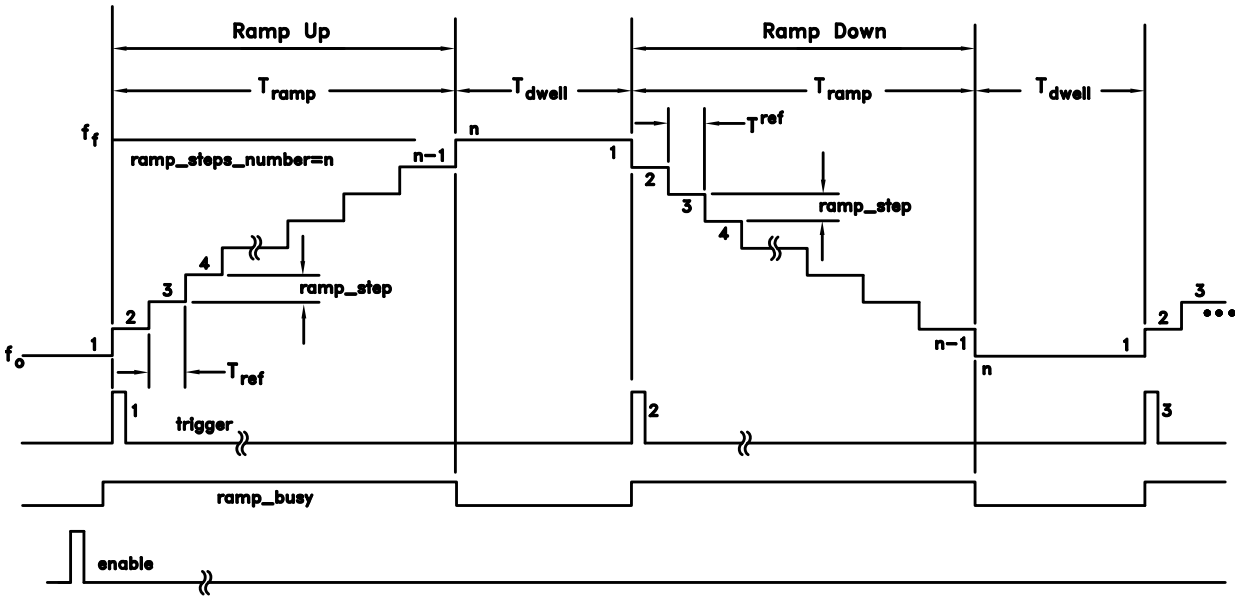

Figure 3. 2-Way Sweep Control via Trigger

4.4.3 Single Step Ramp Mode

Single-step mode is selected by setting ramp_singlestep (Reg 14 h<6>). In this mode, a trigger is required for each step of the ramp. Single-step mode will function with either one-way or two-way ramps. The operation of single-step mode for a one-way ramp is shown graphically in Figure 4.

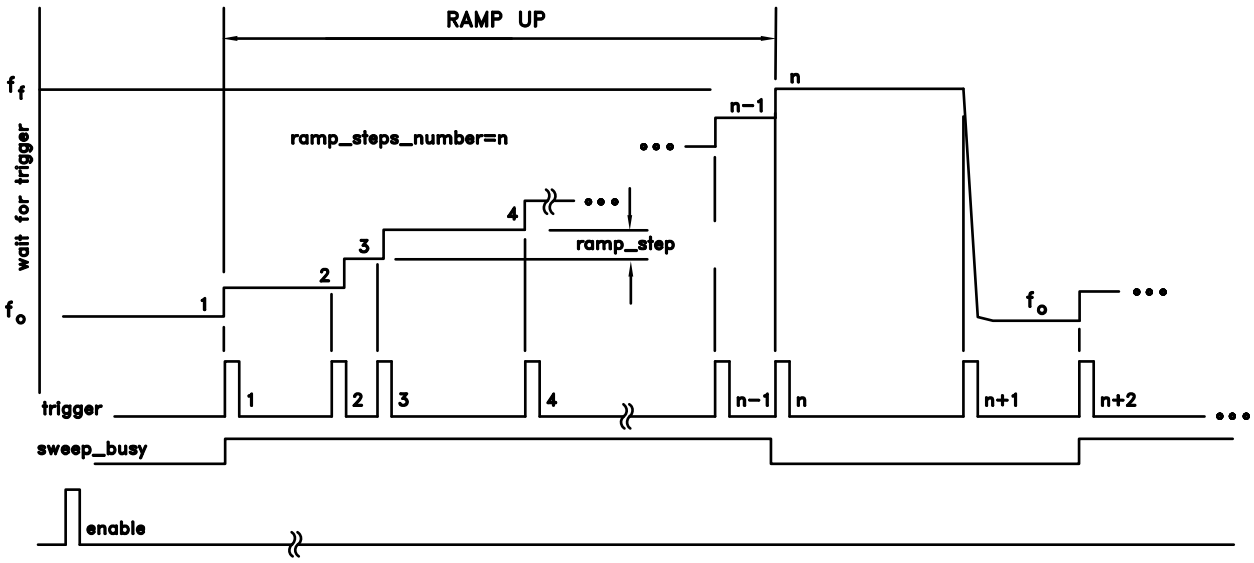

Figure 4. Single Step Ramp Mode

4.4.4 Ramp Busy

In all types of sweeps, ramp_busy will indicate an active sweep and will stay high between the first and nth ramp step. The ramp_busy signal may be monitored one of two ways:

a) ramp_busy is readable via read-only register Reg 1Fh<5>, and

b) ramp_busy may also be monitored on GPIO2 (hardware pin 2) by setting Reg 1B h<3:0> = 8.

4.4.5 Autosweep Mode

The autosweep mode is similar to the two-way sweep shown in (figure) except that triggers are not required. The autosweep mode is enabled by setting ramp_repeat_en (Reg 14 h<3>); once enabled the autosweep initiates the first trigger, steps the number of times given by ramp_steps_number (Reg 16 h) at a rate of one step per divided reference clock cycle. It then waits the dwell time of ramp_dwell_time (Reg 17 h) periods of the divided reference clock, and then automatically triggers the ramp in the opposite direction. The sweep process continues, alternating sweep directions, until disabled.

4.5 Charge Pump

The up and down charge pumps of the synthesizer can each be adjusted to trade between fractional mode spurious levels and phase noise performance. Optimal values will vary across frequency and are best determined empirically for a particular application.

4.5.1 Charge Pump Gain

Up and down charge pump gains are set by cp_UPcurrent_sel and cp_DNcurrent_sel respectively (Reg 07h). Normally the registers are set to the same value. Each of the UP and DN charge pumps consist of 5-bit charge pumps with lsb of 125 µA. The current gain of the pump, in Amps/radian, is equal to the gain setting of this register divided by 2π.

For example if both cp_UPcurrent_sel and cp_DNcurrent_sel are set to ’01000’ h the output current of each pump will be 1 mA and the gain Kp = 1 mA/2π radians, or 159 µA/rad.

Optimum phase noise performance is generally obtained using low gain at lower VCO frequencies and high gain at higher VCO frequencies.

4.5.2 Charge Pump Gain Trim

In most applications Gain Trim is not used. However it is available for special applications.

Each of the UP and DN pumps may be trimmed separately to more precise values to improve current source matching of the UP and DN values, or to allow finer control of pump gain.

The pump trim controls are 3-bits, binary weighted for UP and DN, in cp_UPtrim_sel and cp_DNtrim_sel respectively (Reg 08h). LSB weight is 14.7 µA, 000h = 0 trim, 001h = 14.7 µA added trim, 111 h = 102.9 µA.

4.5.3 Charge Pump Phase Offset

Either of the UP or DN charge pumps may have a DC leakage or “offset” added. The leakage forces the phase detector to operate with a phase offset between the reference and the divided VCO inputs. It is recommended to operate with a phase offset when using fractional mode to reduce non-linear effects from the UP and DN pump mismatch. Phase noise in fractional mode is strongly affected by charge pump offset. In addition, reference spurs in both integer and fractional mode are affected by the offset.

DC leakage or “offset” may be added to the UP or DN pumps using cp_UPoffset_sel and cp_DNoffset_sel (Reg 08h). These are 4 bit registers with 28.7 µA LSB. Maximum offset is 430 µA.

As an example, if the main pump gain was set at 1 mA, an offset of 373 µA would represent a phase offset of about (392/1000)*360 = 133 degrees

4.5.4 Charge Pump Operation Near the Minimum & Maximum Output Frequency

It should be noted that the charge pump is a non-ideal device. Operation of the module tuned to values near the minimum or maximum output frequency results in degradation of the phase noise performance. When operating near the minimum or maximum frequencies, it is recommended to operate the PE11S100X synthesizer modules with a DC leakage that mirrors the direction of frequency offset from center frequency. For example, if the PE11S100X synthesizer modules operates from 5 to 10 GHz, with a center frequency of 7.5 GHz, and the desired frequency of operation is 5.5 GHz, it is recommended to operate with a DC leakage in the down direction. The converse is also true. If operating the module near its maximum frequency, then a DC leakage in the UP direction is recommended. The appropriate leakage value is application dependent and it is left to the user to determine the appropriate setting based on the application requirements.

4.6 Power On Reset (POR)

Normally all logic cells in the internal PLL are reset when the device digital power supply, Vd1, is applied. This is referred to as Power On Reset, or just POR. POR normally takes about 500 us after the Vd1 supply exceeds 1.6 V, guaranteed to be reset in 1 ms. Once the Vd1 supply exceeds 1.6 V, the POR will not reset the digital again unless the supply drops below 800 mV.

4.6.1 Soft Reset

The SPI registers may also be soft reset by an SPI write to strobe global_swrst_regs (Reg 00h<0>).

All other digital items, including the fractional modulator, may be reset with an SPI write to strobe global_swrst_dig (Reg 00h<1>).

4.6.2 Power Down

The internal PLL chip may be powered down by writing a zero to Reg 01h. In power down state, VD1 will draw less than 1 mA. Note that a signal will still be present at the output (frequency may be anywhere in the VCO tune range). It should be noted that Reg 01h is the Enable and Reset Register which controls 16 separate functions in the chip. Depending upon the desired mode of operation of the chip, not all of the functions may be enabled when in operation. Hence power up of the chip requires a selective write to Reg 01h bits. An easy way to return the chip to its prior state after a power down is to first read Reg 01h and save the state, then write a zero to Reg 01h for reset and then simply rewrite the previous value to restore the chip to the desired operating mode.

5.0 Serial Port

The serial port is designed to operate on 3.3 V logic signals. At no time should levels above 3.6 V be applied to these pins.

Typical serial port operation can be run with SCK at speeds up to 50 MHz.

5.1 Serial Port WRITE Operation

Table 1. Timing Characteristics

Parameter	Conditions	Min	Typ	Max	Units
t_1	SEN to SCK Setup Time	8			nsec
t_2	SDI to SCK Setup Time	10			nsec
t_3	SDI to SCK Hold Time	10			nsec
t_4	SCK High Duration	8			nsec
t_5	SCK Low Duration	8			nsec
t_6	SEN High Duration	640			nsec

A typical WRITE cycle is shown in Figure 5.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low initiates the Write cycle (/WR).

c. Host places the six address bits on the next six falling edges of SCK, MSB first.

d. Slave reads the address bits in the next six rising edges of SCK (2-7).

e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first.

f. Slave reads the data bits on the next 24 rising edges of SCK (8-31).

g. SEN is de-asserted on the 32nd falling edge of SCK.

h. The 32nd falling edge of SCK completes the cycle.

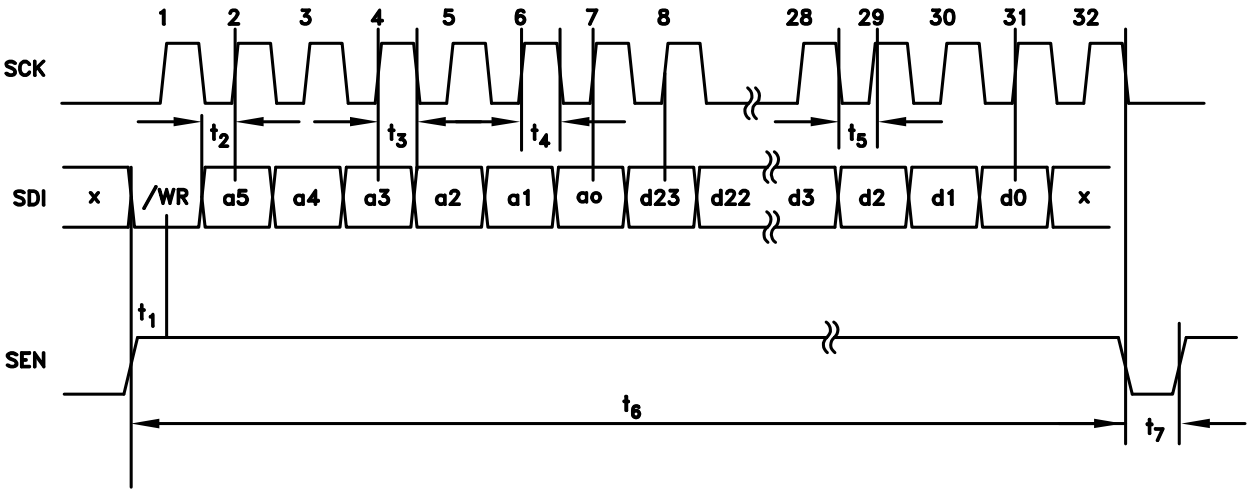

Figure 5. Serial Port Timing Diagram - Write Serial Port WRITE Operation

5.2 Main Serial Port READ Operation

The synthesizer uses the multi-purpose pin, LD, for both Lock Detect and Serial Data Out (SDO) functions. The registers lkd_to_sdo_automux_en (Reg 1Ah<12>) and lkd_to_sdo_always (Reg 1Ah<13>) determine how the Data Output pin is muxed with the Lock Detect function. If both of the registers are cleared, then

the pin is exclusively SDO. If automux is enabled, the pin switches to SDO when the RD function is sensed on the 1st rising edge of SCK. If lkd_to_sdo_always is set, then the pin LD is dedicated for Lock Detect only, and it is not possible to read from the synthesizer.

A typical READ cycle is shown in Figure 6.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCK

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI high initiates the READ cycle (RD)

c. Host places the six address bits on the next six falling edges of SCK, MSB first.

d. Slave reads the address bits on the next six rising edges of SCK (2-7).

e. Slave places the 24 data bits on the next 24 rising edges of SCK (8-31), MSB first.

f. Host reads the data bits on the next 24 falling edges of SCK (8-31).

g. SEN is de-asserted on the 32nd falling edge of SCK.

h. The 32nd falling edge of SCK completes the cycle

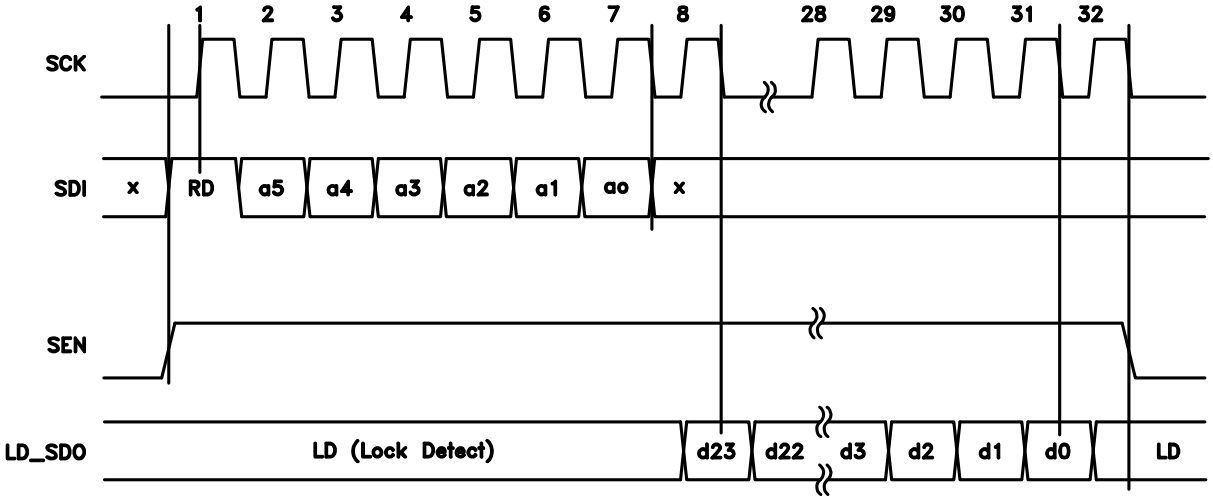

Figure 6. Serial Port Timing Diagram – READ

6.0 Advanced Operation

6.1 Cycle Slip Prevention (CSP)

When changing frequencies the VCO is not yet locked to the reference and the phase difference at the PFD varies rapidly over a range much greater than ±2π radians. Since the gain of the PFD varies linearly with phase up to ±2π, the gain of conventional PFDs will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically as shown in the red curve in Figure 7. Cycle slipping increases the time to lock to a value far greater than that predicted by normal small signal Laplace analysis.

The synthesizer features Cycle Slip Prevention (CSP), an ability to virtually eliminate cycle slipping during acquisition. When enabled, the CSP feature essentially holds the PFD gain at maximum until such time as the frequency difference is near zero. CSP allows significantly faster lock times as shown in Figure 7. The use of the CSP feature is enabled with pfds_rstb (Reg 01h<15>). The CSP feature may be optimized for a given set of PLL dynamics by adjusting the PFD sensitivity to cycle slipping. This is achieved by adjusting pfds_sat_deltaN (Reg 1C h<3:0>).

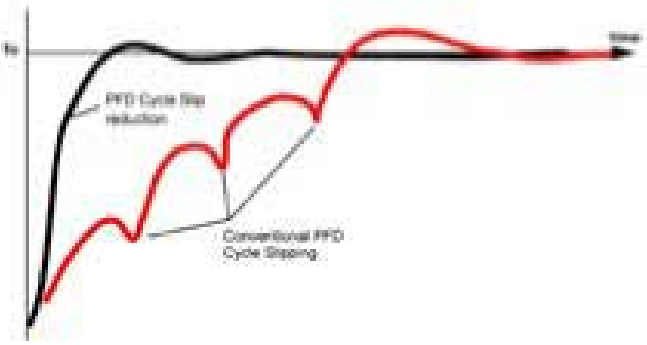

Figure 7. Cycle Slip Prevention (CSP)

6.2 PFD Jitter & Lock Detect Background

In normal phase locked operation, the divided VCO signal arrives at the phase detector in phase with the divided crystal signal, known as the reference signal. Despite the fact that the device is in lock, the phase of the VCO signal and the reference signal vary in time due to the phase noise of the crystal and VCO oscillators, the loop bandwidth used and the presence of fractional modulation or not. The total integrated noise on the VCO path normally dominates the variations in the two arrival times at the phase detector if fractional modulation is turned off.

If we wish to detect if the VCO is in lock or not, we need to distinguish between normal phase jitter when in lock and phase jitter when not in lock.

First, we need to understand what the jitter of the synthesizer is, measured at the phase detector in integer or fractional modes.

The standard deviation of the arrival time of the VCO signal, or the jitter, in integer mode may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi_2(f_o)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade roll off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 8.

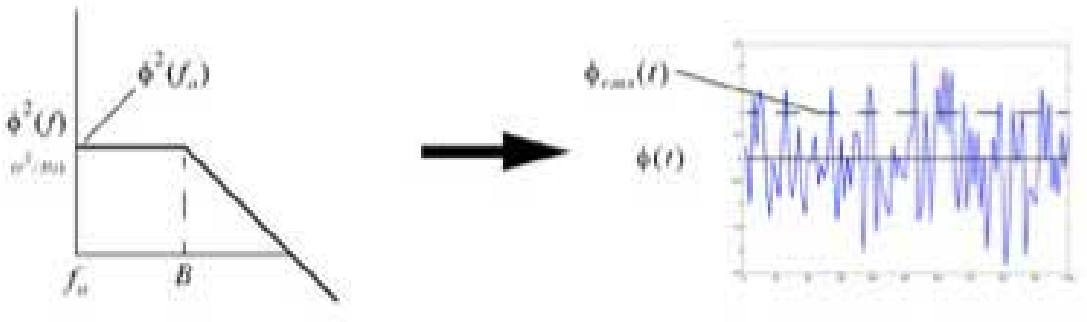

Figure 8. Graphical Representation of Locked VCO Phase Noise in the Frequency & Time Domains

With this simplification the single sideband integrated VCO phase noise, Φ_2, in rads$_2$ at the phase detector is given by

where

$$\Phi^2_{SSB} = (\Phi^2(f_o)\, B\, \pi) / 2\, N^2 \qquad \text{(EQ 2)}$$

$\Phi^2_{SSB}(f_o)$ is the single sideband phase noise in rads$_2$/Hz inside the loop bandwidth, B is the 3-dB corner frequency of the closed loop PLL, and N is the division ratio of the prescaler.

The rms phase jitter of the VCO in rads, Φ, results from the power sum of the two sidebands:

$$\Phi = \sqrt{2\Phi^2_{SSB}} \qquad \text{(EQ 3)}$$

Since the simple integral of (EQ 3) is just a product of constants, we can easily do the integral in the log domain.

For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio N=100, then the integrated single sideband phase noise at the phase detector in dB is given by $\Phi^2_{dB} = 10\log(\Phi^2(f_o)B\pi / N^2) = -100 + 50 + 5 - 40 = -85$ dBrads, or equivalently $\Phi = 10^{-82/20} = 56$ urads rms or 3.2 milli-degrees rms.

While the phase noise reduces by a factor of 20logN after division to the reference, the jitter is a constant. The rms jitter from the phase noise is then given by $T_{jpn} = T_{ref}\,\Phi / 2\pi$

In this example if the reference was 50 MHz, T_{ref} = 20 nsec, and hence T_{jpn} = 178 femtoseconds.

A normal 3 sigma peak-to-peak variation in the arrival time therefore would be $\pm 3\sqrt{2}\, T_{jpn} = 0.756$ ps

If the synthesizer was in fractional mode, the fractional modulation of the VCO divider will dominate the jitter. The exact standard deviation of the divided VCO signal will vary based upon the modulator chosen, however a typical modulator will vary by about ±3 VCO periods, ±4 VCO periods, worst case.

If, for example, a nominal VCO at 5 GHz is divided by 100 to equal the reference at 50 MHz, then the worst case division ratios will vary by 100±4. Hence the peak variation in the arrival times caused by ΔΣ modulation of the fractional synthesizer at the reference will be:

$$T_{j\Delta\Sigma pk} = \pm T_{VCO} \cdot (N_{max} - N_{min}) / 2 \qquad \text{(EQ 4)}$$

In this example, $T_{j\Delta\Sigma pk} = \pm 200$ ps$(104-96)/2 = \pm 800$ ps. If we note that the distribution of the delta sigma modulation is approximately gaussian, we could approximate $T_{j\Delta\Sigma pk}$ as a 3 sigma jitter, and hence we could estimate the rms jitter of the ΔΣ modulator as about 1/3 of $T_{j\Delta\Sigma pk}$ or about 266 ps in this example.

Hence the total rms jitter Tj, expected from the delta sigma modulation plus the phase noise of the VCO would be given by the rms sum, where:

$$T_j = \sqrt{T_{jpn}^{2} + \frac{(T_{j\Delta\Sigma pk})^2}{3}} \qquad \text{(EQ 5)}$$

In this example the jitter contribution of the phase noise calculated previously would add only 0.764psec more jitter at the reference, hence we see that the jitter at the phase detector is dominated by the fractional modulation.

Bottom line, we have to expect about ±0.8 ns of normal variation in the phase detector arrival times when in fractional mode. In addition, lower VCO frequencies with high reference frequencies will have much larger variations. For example, a 1 GHz VCO operating at near the minimum nominal divider ratio of 36, would, according to (EQ 4), exhibit about ±4 ns of peak variation at the phase detector, under normal operation. The lock detect circuit must not confuse this modulation as being out of lock.

6.3 PFD Lock Detect

pfd_lkd_en (Reg 01h<11>) enables the lock detect functions of the Internal PLL.

The Lock Detect circuit in the Internal PLL places a one shot window around the reference. The one shot window may be generated by either an analog one shot circuit or a digital one shot based upon an internal ring oscillator timer. Clearing lkd_ringosc_mono_select (Reg 1A h<14>) will result in a nominal ±10 ns 'analog' window of fixed length, as shown in Figure 3. Setting lkd_ringosc_mono_select will result in a variable length 'digital' widow.

The digital one shot window is controlled by lkd_ringosc_cfg (Reg 1A h<16:15>). The resulting lock detect window period is then generated by the number of ring oscillator periods defined in lkd_monost_duration Reg 1A h<18:17>. The lock detect ring oscillator may be observed on the GPO2 port by setting ringosc_ testmode (Reg 1A h<19>) and configuring the gpo_sel<3:0> = 0111 in Reg 1B h. Lock detect does not function when this test mode is enabled.

lkd_wincnt_max (Reg 1A h<9:0>) defines the number of consecutive counts of the VCO that must land inside the lock detect window to declare lock. If for example we set lkd_wincnt_max = 1000 , then the VCO arrival would have to occur inside the selected lock widow 1000 times in a row to be declared locked. When locked the Lock Detect flag ro_lock_detect (Reg 1Fh<0>) will be set. A single occurrence outside of the window will result in clearing the Lock Detect flag, ro_lock_detect.

The Lock Detect flag ro_lock_detect (Reg 1Fh<0>) is a read only register, readable from the serial port. The Lock Detect flag is also output to the LD pin according to lkd_to_sdo_always (Reg 1A h<13>) and lkd_to_sdo_automux_en (Reg 1A h<12>), both in Table 28. Setting lkd_to_sdo_always will always display the Lock Detect flag on LD. Clearing lkd_to_sdo_always and setting lkd_to_sdo_automux_en will display the Lock Detect flag on LD except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the lock detect function after the read is completed.

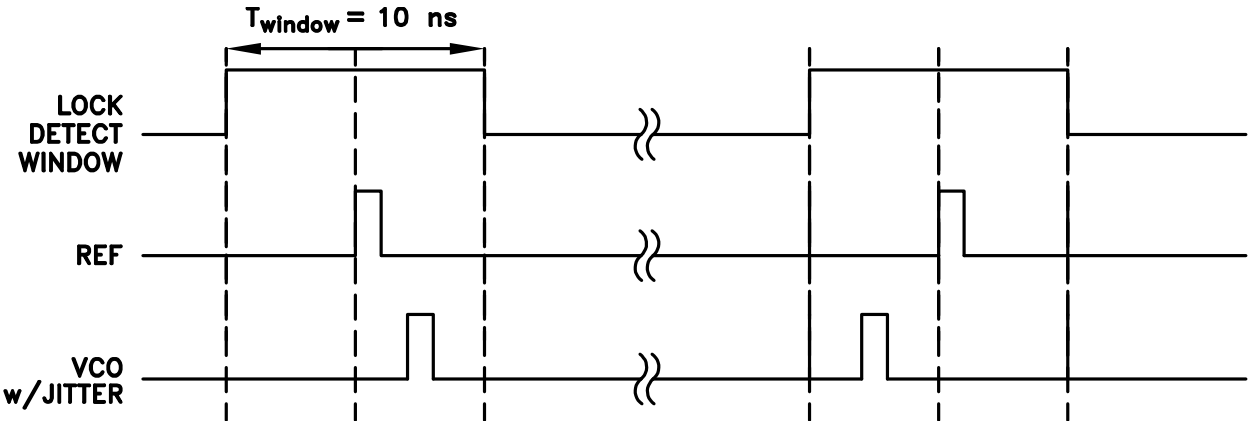

Figure 9. Normal Lock Detect Window

6.4 Lock Detect with Phase Offset

When operating in fractional mode the linearity of the charge pump and phase detector are more critical than in integer mode. The phase detector linearity is worse when operated with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the reference and the VCO at the phase detector. In such a case, for example with an offset delay, as shown in Figure 10, the mean phase of the VCO will always occur after the reference. The lock detect circuit window can be made more selective with a fixed offset delay by setting lkd_win_asym_enable and lkd_win_asym_up_select (Reg 1A h<11>). Similarly the offset can be in advance of the reference by clearing lkd_win_asym_up_select while leaving lkd_win_asym_enable Reg 19 h<10> set. lkd_win_asym_enable is Reg 1A h<10>, lkd_win_asym_up_select is Reg 1A h<11>.

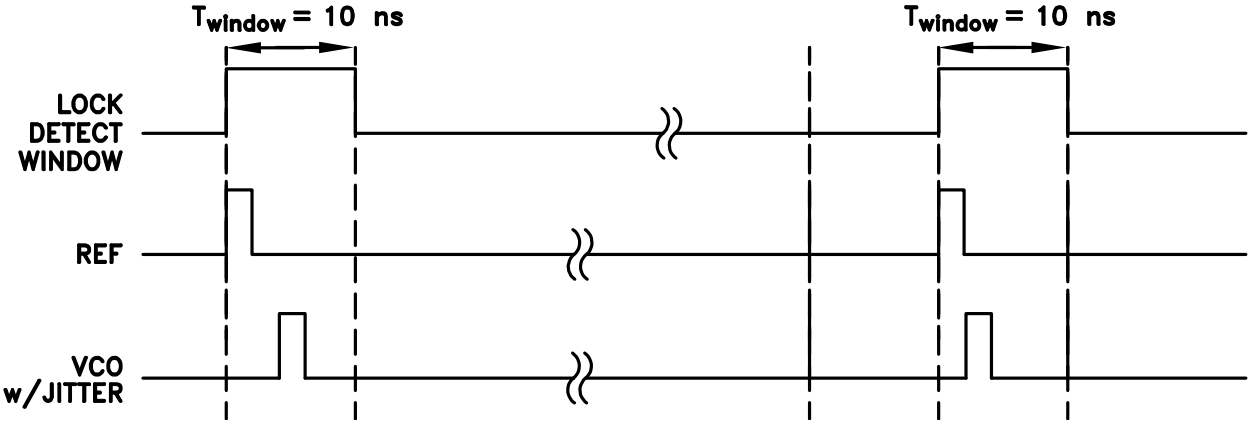

Figure 10. Delayed Lock Detect Window

7.0 Register Map

7.1 Reg 00h Chip ID (Read Only) Register

Bit	Type	Name	Default	Description
[23:0]	Ro	Chip ID	581502h	Chip ID

7.2 Reg 00h Strobe (Write Only) Register

Bit	Type	Name	Default	Description
0	STR	global_swrst_regs	0	Strobe to soft reset the SPI registers
1	STR	global_swrst_dig	0	Strobe to soft reset the rest of digital
2	STR	mcnt_resynch	0	Reserved
3	STR	tsens_spi_strobe	0	Strobe to clock the temp measurement on demand

7.3 Reg 01h Enable & Reset Register

Bit	Type	Name	Default	Description
0	R/W	malg_vcobug_en	1	VCO Buffer Enable
1	R/W	mag_bias_en	1	Bias enable
10:2	R/W	Reserved	479	Reserved
11	R/W	pfd_lkd_en	1	Enable / Resetb to digital lockdetect circuit and PFD's lockdetect output gates
12	R/W	cp_en	1	Charge Pump Enable, disable is tri-stated output
13	R/W	dsm_rstb	0	1 - Enables fractional modulator see also dsm_integer_mode Reg12h<3>
14	R/W	lkd_rstb	1	1 - enables lock detect circuit
15	R/W	pfds_rstb	1	CSP PFD FF rstb 1 - Enables the Cycle Slip Prevention (CSP) feature of the PFD

7.4 Reg 02h Serial Data Out Force Register

Bit	Type	Name	Default	Description
0	R/W	malg_sdo_driver_force_val	1	Serial Data Out Force value This value may be forced onto LD_SDO by setting malg_sdo_driver_force_en
1	R/W	malg_sdo_driver_force_en	1	Serial Data Out EN Force enable Places value from malg_sdo_driver_force_val on SDO

7.5 Reg 03h Reserved

Bit	Type	Name	Default	Description
13:0	R/W	rfp_div_ratio, also referred to as “R”	1	
16:14	R/W	Reserved	7	Reserved

7.6 Reg 04h Prescaler Duty Cycle Register

Bit	Type	Name	Default	Description
0	R/W	vcop_dutycycmode	1	Extends the low time from 15 to 47 VCO cycles for large divide ratios

7.7 Reg 05h Reserved

Bit	Type	Name	Default	Description
2:0	R/W	Reserved	7	Reserved

7.8 Reg 06h Phase Freq Detector Delay Register

Bit	Type	Name	Default	Description
2:0	R/W	pfd_del_sel	2	Delay line setpoint to PFD

7.9 Reg 07h Charge Pump UP/DN Control Register

Bit	Type	Name	Default	Description
4:0	R/W	cp_UPcurrent_sel	16	Sets Charge-Pump Up gain, 125 µA lsb, binary, 4 mA max
9:5	R/W	cp_DNcurrent_sel	16	Sets Charge-Pump Dn gain, 125 µA lsb, binary, 4 mA max

7.10 Reg 08h Charge Pump Trim & Offset Register

Bit	Type	Name	Default	Description
3:0	R/W	cp_UPtrim_sel	0	Trim Up gain, 14.3µA lsb, binary, 100µA max
7:4	R/W	cp_DNtrim_sel	0	Trim Dn gain, 14.3µA lsb, binary, 100µA max

11:8	R/W	cp_UPoffset_sel	3	Up Offset leakage current, 28.7 µA lsb, binary, 430 µA max
15:12	R/W	cp_DNoffset_sel	0	Dn Offset leakage current, 28.7 µA , binary, 430 µA max
17:16	R/W	cp_amp_bias_sel	2	Charge Pump Dummy Branch Op amp bias selection, 100 µA

7.11 Reg 09h Charge Pump EN Register

Bit	Type	Name	Default	Description
0	R/W	cp_pull_updn_en	0	Enables CP UP/Down Control Reg09 [1]
1	R/W	cp_pull_dn_upb	0	0 - Forces Charge Pump Up when Reg09[0]=1 1 - Forces Charge Pump DN when Reg09[0]=1

7.12 Reg 0Ah Reserved

Bit	Type	Name	Default	Description
11:0	R/W	Reserved	68	Reserved

7.13 Reg 0Bh Reserved

Bit	Type	Name	Default	Description
15:0	R/W	Reserved	0	Reserved

7.14 Reg 0Ch Reserved

Bit	Type	Name	Default	Description
13:0	R/W	Reserved	256	Reserved

7.15 Reg 0Dh Reserved

Bit	Type	Name	Default	Description
6:0	R/W	Reserved	32	Reserved

7.16 Reg 0Eh Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	0	Reserved

7.17 Reg 0Fh Integer Division Register

Bit	Type	Name	Default	Description
15:0	R/W	dsm_intg	400	unsigned integer portion of VCO divider value, also known as NINT, see EQ 1

7.18 Reg 10h Fractional Division Register

Bit	Type	Name	Default	Description
23:0	R/W	dsm_frac	0	unsigned integer portion of VCO divider value, also known as NFRAC, see EQ 1

7.19 Reg 11h Speed Register

Bit	Type	Name	Default	Description
23:0	R/W	dsm_seed	3A1953h	unsigned seed value for ΔΣ modulator sets the start phase of the modulator

7.20 Reg 12h Delta Sigma Modulator Register

Bit	Type	Name	Default	Description
0	R/W	dsm_ref_clk_select	0	use reference instead of divider
1	R/W	dsm_invert_clk_sd3	0	invert ΔΣ clk
2	R/W	dsm_invert_clk_rph	1	inverts the ref clock phase
3	R/W	dsm_integer_mode	0	1- enables Integer Mode, bypasses the ΔΣ modulator, leaves it running see also dsm_rstb Reg01h<13> to disable the modulator
4	R/W	Reserved	0	
5	R/W	Reserved	0	
6	R/W	dsm_xref_sin_select	1	when xref is selected specifies that the sine source is used
7	R/W	dsm_autoseed	1	automatic seed load when changing the frac part, uses value in seed

9:8	R/W	dsm_order	2	00-first order 01-second 10-third fb 11-third ff
13:10	R/W	dsm_quant_max	4'b0011	max value allowed out of ΔΣ modulator quantizer limits are +7 to -8, typ ±3 or ±4
17:14	R/W	dsm_quant_min	4'b1100	min value allowed out of ΔΣ modulator quantizer limits are +7 to -8, typ ±3 or ±4

7.21 Reg 13h Reserved

Bit	Type	Name	Default	Description
15:0	R/W	Reserved	0	Reserved

7.22 Reg 14h CW Sweep Control Register

Bit	Type	Name	Default	Description
0	R/W	clear_ovf_undf	0	asynchronous clear for ovf/undf flags
1	R/W	ramp_enable	0	Ramp En/rstb 1= enables the CW Ramp Function
2	R/W	ramp_trigg	0	Write always triggers ramps if bit <2> = 0, if bit <2> = 1, Ramp will not trigger, bit <2> must be reset to 0 first
3	R/W	ramp_repeat_en	0	Ramp Repeat Seq enable 1= enables autotrigger of ramps 0 = ramp_trigg starts each ramp
4	R/W	ramp_startdir_dn	0	Ramp start direction 1= Start with Ramp Down 0= Start with Ramp Up
5	R/W	ramp_trig_ext_en	0	Enable hardware trigger on GPO3 pin
6	R/W	ramp_singlestep	0	Ramp single step, advances the ramp to the next step, and holds frequency
7	R/W	ramp_singledir	0	Ramps in one direction only with hop to start at end of ramp

7.23 Reg 15h CW Sweep Ramp Step Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_step	2048	Ramp Step size

7.24 Reg 16h CW Sweep Ramp Step Number Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_steps_number	2048	Ramp Number of steps in ramp

7.25 Reg 17h CW Sweep Dwell Time Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_dwell_time	2048	Ramp Number of cycles to hold at top/bottom in repeat mode

7.26 Reg 18h Reserved

Bit	Type	Name	Default	Description
22:0	R/W	Reserved	144	Reserved

7.27 Reg 19h Reserved

Bit	Type	Name	Default	Description
4:0	R/W	Reserved	15	Reserved

7.28 Reg 1Ah Lock Detect Register

Bit	Type	Name	Default	Description
9:0	R/W	lkd_wincnt_max	298	threshold count in the timer window to declare lock (reference cycles)
10	R/W	lkd_win_asym_enable	0	Enables asymmetric lock detect window (nominal 10nsec)
11	R/W	lkd_win_asym_up_select	0	Sets polarity of the window
12	R/W	lkd_to_sdo_automux_en	1	Muxes the lkd output signal to SDO when SDO is not being used for Main Serial Port Data Outputs (Read Operation)
13	R/W	lkd_to_sdo_always	0	Muxes the lkd output signal to SDO always, not possible to do Main Serial Port Read in this state
14	R/W	lkd_ringosc_mono_select	0	1 select ringosc based oneshot for lock detect window 0 selects analog based oneshot

16:15	R/W	lkd_ringosc_cfg	3	“0” fastest “3” slowest
18:17	R/W	lkd_monost_duration	3	“0” shortest “3” longest
19	R/W	lkd_ringosc_testmode	0	enables the ring osc by itself for testing

7.29 Reg 1Bh GPO Control Register

Bit	Type	Name	Default	Description
3:0	R/W	gpo_sel	0	Selects data to be driven on GPO ports
		gpo_sel<3:0> = 0000		GPO3 <=gposel_0_data<2> GPO2 <= gposel_0_data<1> GPO1 <= gposel_0_data<0>
		gpo_sel<3:0> = 0001		GPO3 <= xref_clk_in GPO2 <= ref_clk_in GPO1 <= vco_div_clkin
		gpo_sel<3:0> = 0010		GP03 <= pfd_up_in GP02 <= pfd_dn_in GP01 <= LKD_monost_window
		gpo_sel<3:0> = 0011		GP03 <= pfd_sat_ref_in GP02 <= pfd_sat_vco_div_in GP01 <= delta_integer_cycslip_sel, this strobe holds the gain of the PFD at max for anti-cycle slipping
		gpo_sel<3:0> = 0100		GP03 <= xref_clk_in GP02 <= xref_sin_in GP01 <= sd_frac_strobe_sync, internally synchronized frac strobe
		gpo_sel<3:0> = 0101		VCO Serial Port Mirror GPO3 - VSDO GPO2 = VSCK GPO1 = SVLE
		gpo_sel<3:0> = 0110		GP03 <= SD_Intz1<1> GP02 <=SD_Intz1<2> GP01 <= SD_Intz1<3> 3-bit quantized version of the VCO phase
		gpo_sel<3:0> = 0111		GP03 <= aux_clk GP02 <= ringosc_test GP01 <= clk_SD
		gpo_sel<3:0> = 1000		GP03 <= 00 GP02 <= ramp_busy GP01 <= vcot_busy
		gpo_sel<3:0> = 1001		Not used
		gpo_sel<3:0> = 1010		GP03 <= ΔΣ Quantizer Output 3rd lsb GP02 <= ΔΣ Quantizer Output 2nd lsb GP01 <= ΔΣ Quantizer Output lsb
6:4	R/W	gpo_sel_0_data	0	this data is driven on gpo if gpo_sel==0
7	R/W	gpo_dig_drive_en	1	enables Tri-state drivers on GPO output pads
10:8	R/W	Chip ID 478732 Reserved Chip ID 481502 gpo_ind_drive_dis	 0 0 	reserved must write 0 on Chip ID 478732 Chip ID 481502 Only 000 = all GPO pad drivers enabled xx1 = disable GPO1 pad driver

				x1x = disable GPO2 pad driver 1xx = disable GPO3 pad driver

7.30 Reg 1Ch Phase Detector CSP Register

Bit	Type	Name	Default	Description
3:0	R/W	pfds_sat_deltaN	0	0= Cycle Slip Prevention (CSP) disabled 4-bit value to advance or retard phase detector in VCO cycles if it reaches 2pi, i.e. cycle slip prevention. 1st bit is polarity, enabled by rstb
4	R/W	pfds_rstb_force	0	CSP PFD Flip-flops RSTB: 1 - controlled by the pfds_rstb bit: 0 - auto-controlled by the CSP logic Forces the PFD into reset, which tristates charge pump, freezes charge on the loop filter, and hence opens the loop
5	R/W	pfds_rstb	1	CSP PFD FF rstb 1 - Enables the Cycle Slip Prevention (CSP) feature of the PFD

7.31 Reg 1Dh VCO Tune Port Control Register

Bit	Type	Name	Default	Description
0	R/W	voltage_force	1	Selects the source of control of the timing of the mid-rail voltage, voltage_force=0 selects Autotune state machine voltage_force=1 selects voltage_enable from SPI Used for mid-rail control of VCO during autotuning
1	R/W	voltage_enable	0	Forces mid-rail voltage on the charge pump output from the SPI when voltage_force=1 Used for mid-rail control of VCO during autotuning

7.32 Reg 1Eh Temperature Sensor Register

Bit	Type	Name	Default	Description
0	R/W	tsens_spi_enable	0	Enable the temperature sensor, draws ~2mA current, must strobe tsens_spi_strobe Reg 00h <3>

7.33 Reg 1Fh LD, VCO & Ramp Busy Read Only Register

Bit	Type	Name	Default	Description
0	RO	ro_lock_detect	1	1 = locked, 0 = unlocked
3:1	RO	ro_dsm_overflow	0	1 = modulator overflow
4	RO	ro_spi_vco_busy	0	Set when VCO autotuning is running
5	RO	ro_ramp_busy	0	Sweeper status flag, set when ramp is busy, cleared when at end of ramp or not used

7.34 Reg 20h Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	32	Reserved

7.35 Reg 21h Temperature Sensor Read Only Register

Bit	Type	Name	Default	Description
6:0	RO	tsens_temperature	0	Current Temperature from temp sensor each bit adds 17.5 °C 0000000: Temp < = -22.5 °C 0000001: -22.5 °C < Temp < -5 °C 0000011: -5 °C < Temp < 12.5 °C 0000111: 12.5 °C <Temp < 30 °C 0001111: 30 °C < Temp < 47.5 °C 0011111: 47.5 °C < Temp < 65 °C 0111111: 65 °C < Temp < 82.5 °C 1111111: Temp < 82.5 °C

Resources

Datasheets

https://www.pasternack.com/images/ProductPDF/PE11S1001.pdf

https://www.pasternack.com/images/ProductPDF/PE11S1002.pdf

Website

https://www.pasternack.com/nsearch.aspx?Category=Synthesizers&sort=y&initial_sort=Sortsku:ASC&res_per_page=48&view_type=grid

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